Remarks

I. Status of Claims

Claims 1-13 have been amended.

Claims 14-21 have been withdrawn.

Claims 22-25 have been added.

II. Claim Rejections

A. Independent Claim 1

Independent claim 1 has been amended and now recites that alignment between the integrated chip substrates is within a first alignment tolerance range and alignment between the integrated structures supported by the integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range.

The Examiner has rejected independent claim 1 under 35 U.S.C. § 103(a) over Ho (U.S. 4,254,445) in view of Ferri (U.S. 4,326,180) and Houston (U.S. 6,362,117). The cited references, however, taken alone or in any permissible combination, do not teach or suggest all of the features of the inventive common carrier now recited in independent claim 1. It is noted that the Examiner's discussion regarding the construction of product by process claims does not apply to independent claim 1 as amended because the claim is not defined with respect to any process.

Ho

Ho fails to teach or suggest a common carrier in which alignment between the integrated chip substrates is within a first alignment tolerance range and alignment between the integrated structures supported by the integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range, as now recited in independent claim 1. Indeed, in Ho's approach, integrated structures are formed on substrates to form LSI chips, and the LSI chips subsequently are mounted in package modules. Accordingly, alignment between the integrated structures of the LSI chips is within a larger alignment tolerance range than the alignment between the substrates of the LSI chips because of the accumulation of alignment errors.

Ferri

Ferri discloses a microwave backdiode microcircuit that includes a single diode assembly chip 20 mounted on a dielectric substrate 14. Accordingly, Ferri does not teach or suggest anything about the alignment between a plurality of integrated chip substrates, nor

anything about the alignment between integrated structures supported by respective integrated chip substrates.

Houston

Houston merely discloses a method of making a single integrated circuit chip. Accordingly, like Ferri, Houston does not teach or suggest anything about the alignment between a plurality of integrated chip substrates, nor anything about the alignment between integrated structures supported by respective integrated chip substrates.

B. Dependent Claims 2-13 and 22-25

1. Claim 2

The Examiner has rejected claim 2 under 35 U.S.C. § 103(a) over Ho in view of Ferri, Houston, and Yao (U.S. 6,163,068). The Examiner has cited Yao for his disclosure of "integrated circuit chips 30 adhered to a carrier substrate 20 using an adhesive." Yao, however, like Ho, fails to teach or suggest a common carrier in which alignment between the integrated chip substrates is within a first alignment tolerance range and alignment between the integrated structures supported by the integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range, as now recited in independent claim 1. Indeed, in Yao's approach, integrated structures are formed on substrates to form chips 30, and chips 30 subsequently are mounted to substrate 20. Accordingly, alignment between the integrated structures of the chips 30 is within a larger alignment tolerance range than the alignment between the substrates of the chips 30 because of the accumulation of alignment errors.

Thus, dependent claim 2 is patentable for at least the same reasons as independent claim 1. It is noted that Yao fails to disclose the composition of the double-sided adhesive means 50.

2. Claim 3

The Examiner has rejected claim 3 under 35 U.S.C. § 103(a) over Ho in view of Ferri, Houston, and Akram (U.S. 2001/0014488). The Examiner has cited Akram for his disclosure of "a carrier substrate 102, an adhesive 112, and an integrated circuit chip 104." Akram, however, like Ho, fails to teach or suggest a common carrier in which alignment between integrated chip substrates is within a first alignment tolerance range and alignment between integrated structures supported by the integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range, as recited in independent

claim 1. Indeed, in Akram's approach, integrated structures are formed on substrates to form chips 104, and the chips 104 subsequently are mounted to substrate 102. Accordingly, alignment between the integrated structures of the integrated circuit chips is within a larger alignment tolerance range than the alignment between the substrates of the integrated circuit chips because of the accumulation of alignment errors.

Thus, dependent claim 3 is patentable for at least the same reasons as independent claim 1.

3. Claims 4-9 and 12-13

The Examiner has rejected claims 4-9 and 12-13 under 35 U.S.C. § 103(a) over Ho in view of Ferri and Houston. Claims 4-9 and 12-13 incorporate the features of independent claim 1 and therefore are patentable for at least the same reasons explained above. Claims 5, 6, and 13 also are patentable for the following additional reasons.

Claim 5 recites that the carrier substrate includes a plurality of slots each containing a respective integrated chip. The Examiner has asserted that Ho's "carrier substrate includes a plurality of slots 11." Contrary to the Examiner's assertion, however, the elements 11 of Ho's package module are merely square peripheral areas 11 of substrate 9 that are used "for the fan-out of connections to pads for engineering change connections and for testing" (col. 2, lines 66-67). The peripheral areas 11 are not slots that contain respective integrated chips. For at least this additional reason, the Examiner's rejection of claim 5 under 35 U.S.C. § 103(a) over Ho in view of Ferri and Houston should be withdrawn.

Claim 6 incorporates the features of dependent claim 5 and therefore is patentable for at least the same reasons. Claim 6 additionally recites that the upper surface of the carrier substrate and upper surfaces of the integrated chips are substantially coplanar. The Examiner has asserted that "Ho further teach that the carrier substrate and the integrated chips each having parallel top surfaces which reside essentially within the same plane (Figure 1) and the carrier substrate and the integrated chips each having parallel top surfaces which do not reside within the same plane (Figure 3)." Figures 1 and 3 are top views of package modules and, therefore, do not show anything about whether or not the upper surfaces of chips 10 and the upper surface of substrate 9 are coplanar. Nevertheless, contrary to the Examiner's assertion, Ho clearly teaches that each chip 10 is mounted on substrate 9 (see, e.g., col. 2, lines 63-65). Therefore, the upper surfaces of chips 10 and the upper surface of substrate 9 necessarily are not substantially coplanar. For at least this additional reason, the Examiner's

rejection of claim 6 under 35 U.S.C. § 103(a) over Ho in view of Ferri and Houston should be withdrawn.

Claim 13 recites that each of the plurality of integrated chips is a component of a respective inkjet print head. None of the cited references teaches of suggests such a feature. For at least this additional reason, the Examiner's rejection of claim 13 under 35 U.S.C. § 103(a) over Ho in view of Ferri and Houston should be withdrawn.

4. Claim 10

The Examiner has rejected claim 10 under 35 U.S.C. § 103(a) over Ho in view of Ferri, Houston, and Bayan (U.S. 6,372,359). Claim 10 incorporates the features of independent claim 1 and dependent claim 5 and, therefore, is patentable for at least the same reasons explained above. Claim 10 also is patentable for the following additional reason.

The Examiner has cited Bayan for the disclosure of "a filler material 225 adapted to fill a peripheral gap between the interior edges of each of the slots 208 and the peripheral edges of each of the integrated chips 220 when each chip is adhered within each slot." Claim 10, however, requires that each slot contain a respective integrated chip. In Bayan's approach, none of the dice 220 is contained within a trough 208. Accordingly, in Bayan's approach, there is no "filler material disposed in each peripheral gap between interior edges of each slot and peripheral edges of each respectively contained integrated chip," as now recited in claim 10.

For at least this additional reason, the Examiner's rejection of claim 10 under 35 U.S.C. § 103(a) over Ho in view of Ferri, Houston, and Bayan should be withdrawn.

5. Claim 11

The Examiner has rejected claim 11 under 35 U.S.C. § 103(a) over Ho in view of Ferri, Houston, and Moser (U.S. 4,797,780). Claim 11 incorporates the features of independent claim 1 and dependent claims 5 and 10 and, therefore, is patentable for at least the same reasons explained above. The Examiner has cited Moser for teaching "a filler material comprising glass frit." Moser, however, fails to make up for the failure of Ho, Ferri, Houston, and Bayan to teach or suggest the invention recited in claim 10, as explained above. For at least this reason, the Examiner's rejection of claim 11 under 35 U.S.C. § 103(a) over Ho in view of Ferri, Houston, and Moser should be withdrawn.

III. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

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Respectfully submitted,

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